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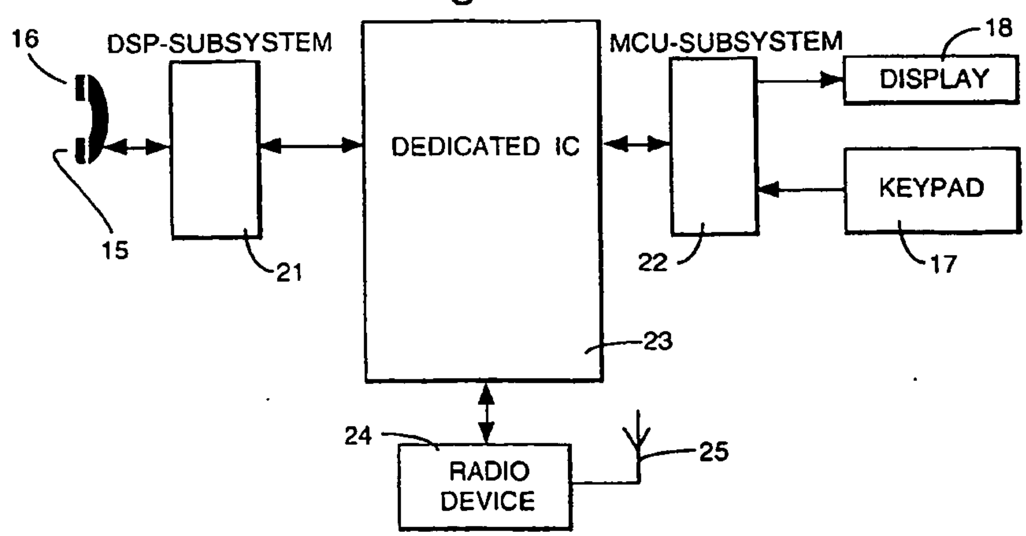
(54) Data buffering device between communicating processors in a cellular mobile telephone terminal.

(57) A data buffering device (33) is positionable between communicating processors (21, 22). At least one of the processors is battery powered and is arranged to be placed in a stand-by condition when not required to process information, thereby reducing overall power consumption.

The data buffering device includes data storage locations (34,41) and means (42, 43) for addressing these locations to effect the transfer of data to or from the memory locations. In addition, interrupting means (42, F1, F2, G1) are provided for generating interrupt signals arranged to interrupt at least one of the processors. Thus, upon receiving an interrupt signal, a communicating processor is switched from its stand-by mode to an active mode and data transfer is effected.

Data transfer may take place in both directions and respective buffering means, with respective interrupt signal generating means, are provided. The device may be used in a mobile cellular telephone, positioned between a controller and a digital signal processor.

Fig.2.



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The present invention relates to providing communication between communicating processors.

With the growing tendency of data processing equipment to become smaller and smaller, it is possible to provide portable machines with ever increasing levels of sophistication. In addition to conventional computer systems, often sold as "lap-tops" and "palm-tops", other equipment, traditionally portable by nature, is making increasing use of digital processing technology. Thus, the new generation of mobile cellular telephones employ digital coding for the transmission and reception of speech signals in addition to digital signal processing within the control environment.

Although the manipulation of signals within the digital domain provides many advantages, a disadvantage of such processing, when compared to analogue processing, is that there tends to be an increased power demand. Clearly, in portable systems, power is supplied from battery packs and any measures which can be invoked to reduce power demand will, for a given size of battery, increase operating time.

In data processing environments, particularly when powered from local power suppliers such as batteries, it is know to deactivate or de-energise processors when these processors are not actually required to perform a data processing function, thereby reducing demands on power consumption. However, as will be appreciated, care must be taken to ensure that, when required, a processor is re-activated, thereby ensuring that a processor does not remain in its "stand-by" state when required to perform a processing operation.

A problem of this nature arises when a first processor is required to communicate with a second processor. In a cellular mobile telephone, a first processor is provided to perform control functions and a second processor, which communicates with said first processor, is provided to perform data signal processing, particularly in connection with the processing of speech signals. Both of these processors draw significant amounts of power from the batteries, therefore it is desirable to place these processors into a "stand-by" state when they are not required to process information. However, it is also essential that these processors are not in their stand-by state when required to receive or transmit information from or to other processors.

According to a first aspect of the present invention, there is provided a data buffering device positionable between processors to provide a communicating means between said processors, comprising data storage location; a register indicating whether said data storage locations have data stored therein to be read out or whether said locations are available for data to be written thereto; and interrupt generating means arranged to generate an interrupt signal to a receiving processor when said register is set to indicate that said locations contain data to be read by said receiving processor.

In a preferred embodiment, interrupt generating means are also provided to supply an interrupt signal to the transmitting processor when said register is reset to indicate that new data may be written to said locations.

Preferably, a first set of storage locations are provided for transferring data from a first processor to a second processor and a second set of storage locations are provided to effect transfer from said second processor to said first processor.

According to a second aspect of the present invention, there is provided a system for providing buffered communication between processors, comprising a first processor having an operational condition and a power-saving stand-by condition and a second processor; data storage locations providing buffer storage between the processors; interrupt generating circuitry arranged to interrupt one of the processors in response to a state change in the register caused by the other processor.

According to a third aspect of the present invention, there is provided a method of providing communication between a first processor having a power-saving stand-by condition and an operational condition and a second processor via mutually accessible data storage locations involving the steps of:

(i) the second processor accessing the data storage locations;

(ii) the second processor generating an interrupt after said accessing step is complete; and

(iii) the first processor responding to the interrupt by switching from its stand-by to its operational condition to allow for access to the data storage locations.

Subsidiary features of the present invention are given in the appended claims.

The invention will now be described by way of example only, with reference to the accompanying drawings in which;

Figure 1 shows a mobile telephone having an output loud speaker, an input microphone, a menu display and a battery pack;

Figure 2 is a schematic representation of the telephone shown in Figure 1, including a digital signal processing subsystem, a micro controlling unit subsystem and a dedicated integrated circuit facilitating the transfer of data from between said subsystems;

Figure 3 details the dedicated integrated circuit shown in Figure 2, including random access memory devices and control circuits; and

Figure 4 details a control circuit of the type shown in Figure 3.

A mobile telephone is shown in Figure 1, having a mouthpiece microphone 15 and an earpiece loud-

speaker 16. Conventional signalling buttons 17 are provided, enabling telephone numbers to be dialled and supplementary telephony services to be effected using the star and square buttons. A liquid crystal display 18 also provides a visual display to an operator which, in addition to facilitating conventional telephony operations, also assist the operator in the selection of other operating characteristics.

In operation, the telephone shown in Figure 1 performs a significant degree of data processing, in order to facilitate communication with base stations using digital coding techniques.

All of the processing performed by the telephone shown in Figure 1 is powered by means of a local battery pack 19, which would normally be provided with sufficient energy to power the telephone in a fully operational way for several hours, between re-charges.

As will be appreciated, the conversion of analogue speech signals into a digitally encoded signals along with the reverse process when receiving signals, requires a considerable processing overhead. Processing of the speech signals is effected using a dedicated digital signal processor within the telephone housing shown in Figure 1. Similarly, a significant degree of control and signalling is required and again a dedicated microcomputer control unit is provided to facilitate the control functions within the telephone. Thus, to a large extent, each of these processing domains remain separate, each being allocated specific tasks within the communicating environment. However, it is also necessary, on occasions, for the microcomputer control unit to communicate with the digital signal processor.

In practice, the digital signal processor will tend to operate at a much faster rate than the microcomputer control unit, allowing power savings to be made by effectively placing said control unit in a stand-by condition, awaiting data to be processed by the digital signal processor before commencing its next task. However, a problem arises in that, once placed in its stand-by condition, action must be taken to ensure that it is placed in its active condition prior to effecting a data transfer with the digital signal processor. Furthermore, it would be undesirable to burden the digital signal processor with the additional task of ensuring that the microcomputer control unit is in a suitable condition for communicating, prior to that communication taking place.

A schematic representation of the telephone shown in Figure 1 is presented in Figure 2. Mouthpiece 15 and earpiece 16 communicate with a digital processing subsystem 21. Subsystem 21 includes a conventional digital signal processor, such as a DSP1616 supplied by AT&T.

Signals generated in response to the depression of key 17, result in signals being supplied to a micro control unit subsystem 22, including a conventional microprocessor such as an H8/536 applied by Hitachi. In addition, the micro controller unit subsystem is also arranged to supply signals to display device 18. Additional facilities are provided by a purpose-built dedicated integrated circuit 23, including circuitry for effecting transfers of data between the data signal processing subsystem 21 and the micro control unit subsystem 22.

The integrated circuit 23 also provides an interface to a radio device 24, arranged to modulate signals for transmission to an antenna 25 and to demodulate signals received from the antenna.

Part of the dedicated integrated circuit 23, for effecting the transfer of data between the DSP subsystem 21 and the MCU subsystem 22, is detailed in Figure 3. The integrated circuit 23 is connected to the bus lines 31 of the DSP subsystem 21 and connected to the bus lines 32 of the micro control unit subsystem. 22. In order to effect the transfer of data from the DSP subsystem to the MCU subsystem, data is written to storage locations in the form of a random access memory device 33, under the control of a control circuit 34. After the data has been written to the device 33, it may then be read by the MCU subsystem 22, again under the control of the control circuit 34.

A similar arrangement is provided to effect transfer from the MCU subsystem 22 to the DSP subsystem 21. Thus, under the control of a control circuit 35, data is written to storage locations 36 whereafter, again under the control of the control circuit 35, data is read from the storage locations 36 to the DSP subsystem 21, by its respective bus lines 31.

Transmissions between the DSP 21 and the MCU 22 occur in blocks of 68 8-bit bytes and transmission tends to occur every 10 milliseconds. Notwithstanding requirements to perform other processing functions, devices 21 and 22 are placed in non-active stand-by condition when not required to communicate with each other, thereby conserving battery power.

Thus, the dedicated integrated circuit 23 effectively provides a buffering device which is positioned between a first processor 21 and a second processor 22. A buffering device includes data storage locations in the form of memory device 33 for data transfers from the first processor to the second processor and memory device 36 for transfers from the second processor to the first processor. Transfers are effected under the control of control circuit 34. Control circuit 34 includes a register which indicates whether its respective data storage locations have data stored therein to be read out and supplied to the second processor 22. Alternatively, the register indicates whether said locations are available for data to be written thereto from the first processor 21. In addition, the control circuit 34 also includes means for generating interrupt signals arranged to supply an interrupt signal to the receiving second processor 22 when the register has been set to indicate that storage loca-

tions contain data which is to be read by the receiving processor. Furthermore, the control circuit 34 also includes interrupt generating means arranged to generate an interrupt signal to the transmitting processor 21 when the register has been re-set to indicate that the storage locations are available for data to be written thereto.

The buffer may be referred to as a mailbox because it allows either processor to remain in a stand-by condition or "sleep mode" while the other is writing data to or reading data therefrom. When data has been read from the mailbox, an interrupt signal is supplied to the transmitting processor, effectively instructing the processor to transmit its next message. Similarly, when data has been written to the mailbox, the receiving processor is interrupted, thereby instructing it to the effect that a complete message is present which is waiting to be read.

A control circuit, such as control circuit 34 or control circuit 35 is detailed in Figure 4. The control circuit includes a register 41 referred to as the A to B full register, which is set when its respective storage locations are full with data which has been received from the transmitting processor. Thus, when the device shown in Figure 4 represents control circuit 34, the DSP subsystem 21 becomes processor A and the MCU subsystem 22 becomes processor B. Similarly, when representing control circuit 35, these roles are reversed, such that processor A is the MCU subsystem 22 and processor B is the DSP subsystem 21.

The circuitry shown in Figure 4 is arranged to transfer data from processor A to processor B. Processor A is capable of addressing the A to B full register 41 by issuing a specified address on its address bus, which is interpreted by address decoding logic 42. In response to the specific address being supplied to the address decoding logic 42 and provided that the signal on WS line 44 is set low ("0"), the data bit level stored in the register 41 is supplied to the data line of processor A, thereby informing processor A that the buffer is full, register set to logic 1, or that buffer is empty, register 41 set to logic 0.

If a logic level 0 is returned to processor A on interrogation of the register 41, processor A sets the register by writing a logic 1 to it.

The value written to the register 41 by processor A is resynchronised to the system clock of the integrated circuit 23 by 2 flip flops F1 and F2 in association with gate G1. Thus, gate G1 provides a logic level 1 output when a first non-inverting input is at logic level 1 and the second inverting input is at logic level 0. Under this condition, gate G1 produces a pulse which is high for one system clock cycle, shortly after register 41 has been set.

The pulse generated by gate G1 provides an interrupt to processor B. Processor B may have been placed in its sleep condition, so as to save power. Thus, processor B is arranged such that on receiving an interrupt signal it is interrupted from its sleep condition and arranged to call a sub-routine, which in turn effects the reading of data from the storage locations.

Once data has been read from the storage locations, processor B resets the A to B full register 41, by issuing a specific address which is decoded by address decoding logic 43. In response to logic circuit 43 being addressed and provided that the signal on WS line 45 is set high ("1"), gate G2 generates a re-set pulse which asynchronously re-sets register 41. This again causes the logic level stored within the register 41, in this case logic level 0, to propagate through flip flops F1 and F2. Consequently, gate 3 will produce a pulse which is high for one system clock cycle. This pulse interrupts processor A, which itself may have been placed into its sleep mode while waiting for processor B to read data from the mailbox.

When processor A is writing, the output from gate G4 is set to logic 0, hence gate D1 does not drive the databus to the processor. Similarly, when processor B is writing, the outputs of gate G5 is logic level 0, so that line D2 does not drive the databus to processor B.

In theory, the facility exists for either processor to read the A to B full register 41 at any time. The processors may be prevented from accessing the register at particular times, by placing exception conditions within their respective programmes, thereby ensuring that deadlock conditions are avoided.

Claims

1. A data buffering device positionable between processors to provide a communicating means between said processors, comprising
   data storage locations (33, 36);
   a register (41) indicating whether said data storage locations have data stored therein to be read out or whether said locations are available for data to be written thereto; and
   interrupt generating means (42, F1, F2, G1) arranged to supply an interrupt signal to a receiving processor when said register is set to indicate that said locations contain data to be read by said receiving processor.

2. A device according to claim 1, including interrupt generating means (43, G2) arranged to supply an interrupt signal to the transmitting processor when said register is re-set to indicate that said locations have been read.

3. A device according to claim 1 or claim 2, wherein said storage locations include a first set of storage locations for storing data transferred from a first processor to a second processor and a second set of locations arranged to store data trans-

ferred from said second processor to said first processor.

4. A device according to claim 3, wherein each of said sets of storage locations has a respective register and respective interrupt generating means.

5. A device according to any of claims 1 to 4, wherein said receiving processor is arranged to be placed in a stand-by condition, wherein said processor is interrupted from said stand-by condition upon receiving an interrupt signal.

6. A device according to claim 5; wherein said receiving processor is battery operated.

7. A device according to any of claims 1 to 6, wherein said transmitting processor is arranged to enter a stand-by condition and arranged to be interrupted from said stand-by condition on receiving an interrupt signal.

8. A device according to claim 7, wherein said transmitting processor is battery operated.

9. A device according to any of claims 1 to 8, wherein data is transferred in units of 68 bytes.

10. A device according to any of claims 1 to 9, wherein said first processor is a signal processing unit.

11. A device according to any of claims 1 to 10, wherein said second processor is a micro controlling unit.

12. A system for providing buffered communication between processors, comprising:
a first processor having an operational condition and a power-saving stand-by condition and a second processor;
data storage locations providing buffer storage between the processors; interrupt generating circuitry arranged to interrupt one of the processors in response to a state change in the register caused by the other processor.

13. A system according to claim 12, wherein the interrupt generating circuitry is able to initiate the switching of the first processor from its stand-by mode to its operational mode.

14. A method of providing communication between a first processor having a power-saving stand-by condition and an operational condition and a second processor via mutually accessible data storage locations involving the steps of:
(i) the second processor accessing the data storage locations;
(ii) the second processor generating an interrupt after said accessing step is complete; and
(iii) the first processor responding to the interrupt by switching from its stand-by to its operational condition to allow for access to the data storage locations.

Fig.1.

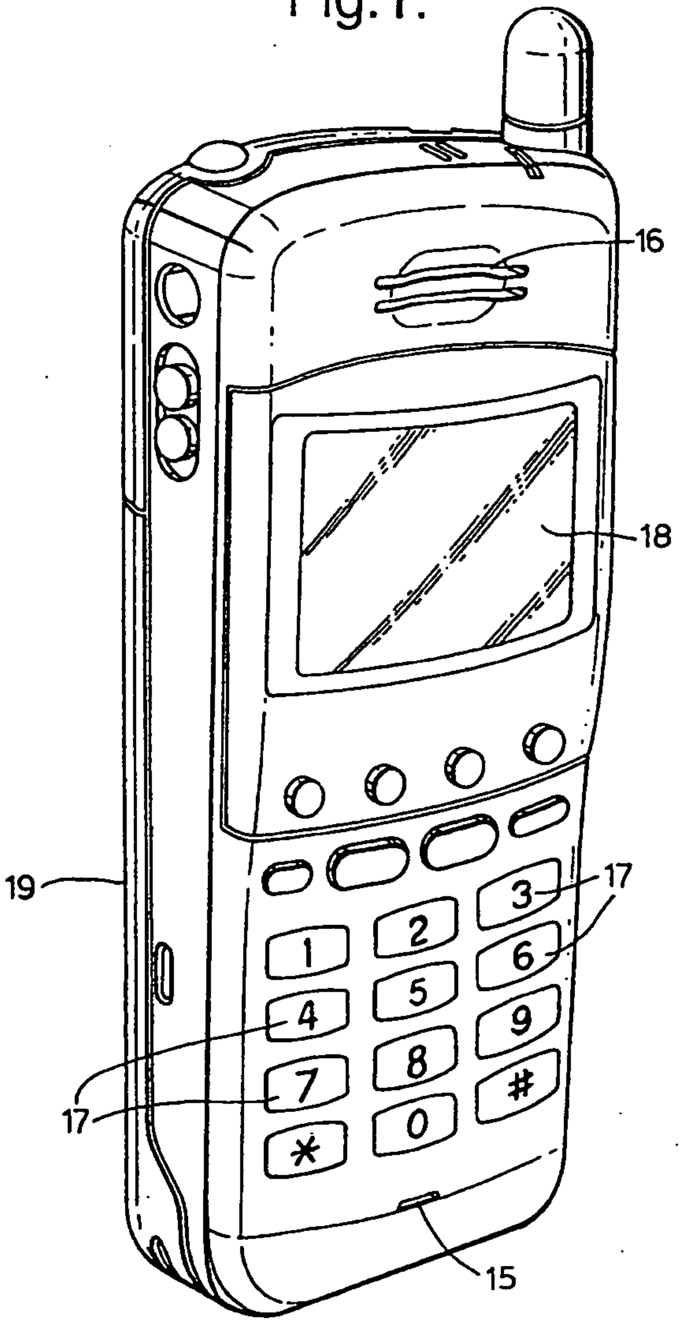


Fig.2.

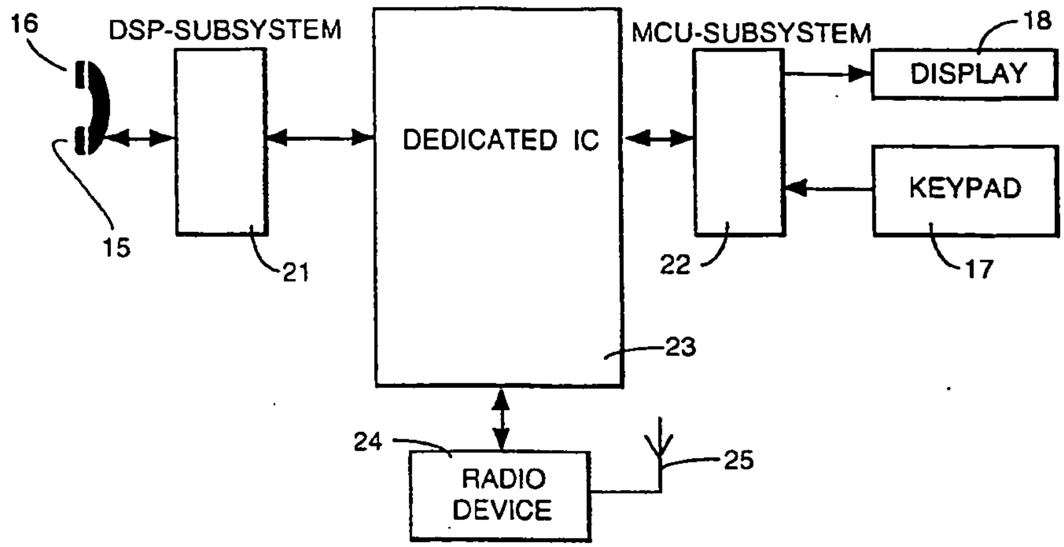
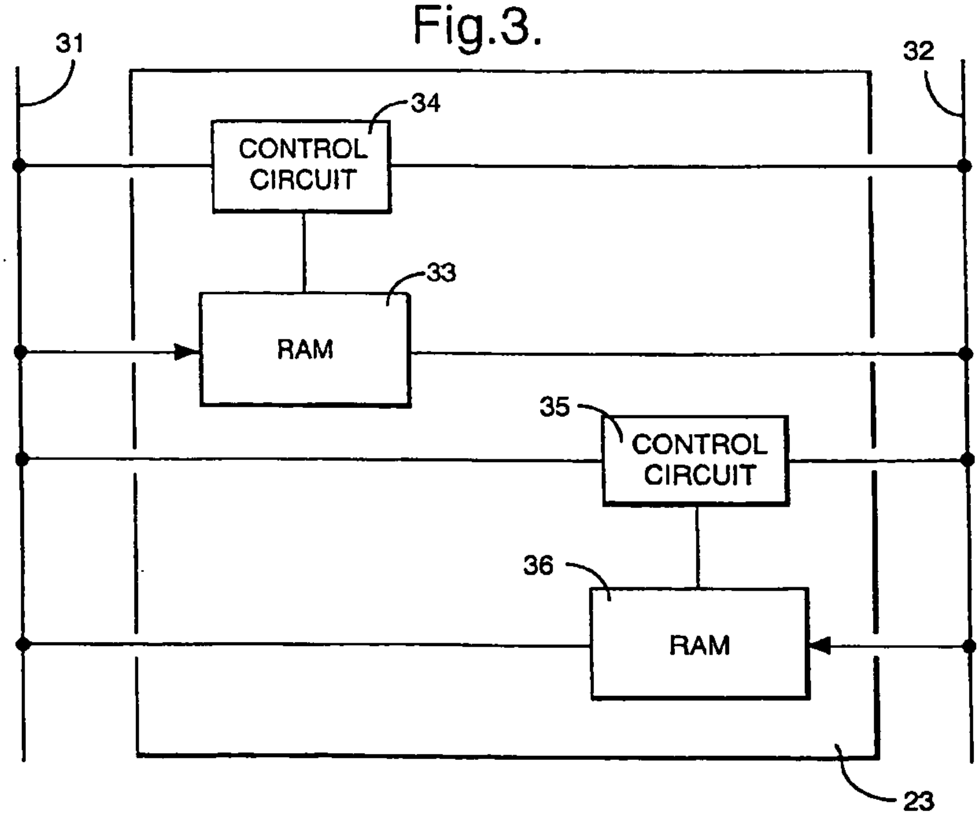

16
DSP-SUBSYSTEM
DEDICATED IC
MCU-SUBSYSTEM
18
DISPLAY
KEYPAD
15
21
22
17
23
24
RADIO DEVICE
25

Fig.3.


31
32
34
CONTROL CIRCUIT
33
RAM
35
CONTROL CIRCUIT
36
RAM
23

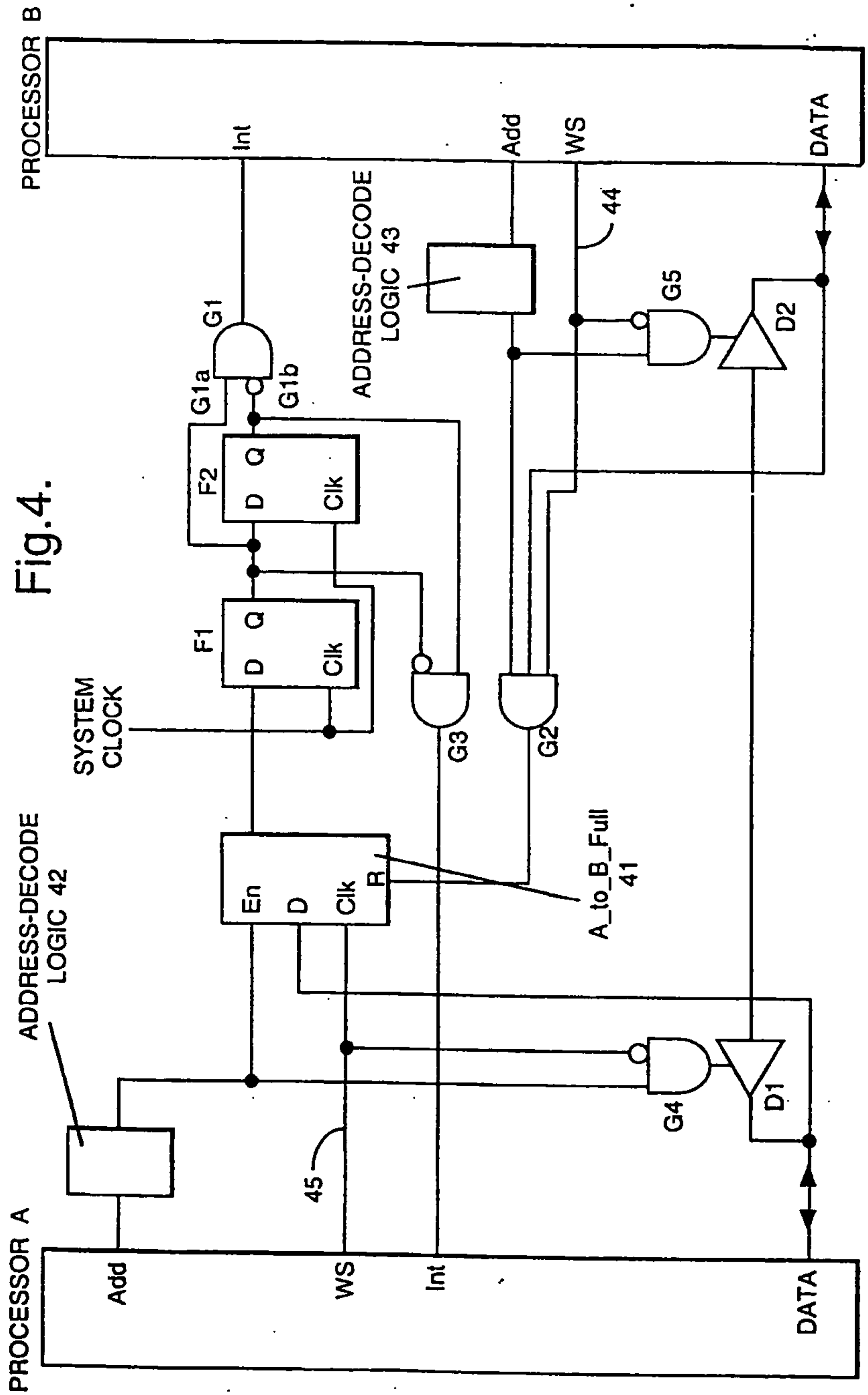

PROCESSOR B
Int
Add
WS
DATA
ADDRESS-DECODE LOGIC 43
44
G1
G1a
G1b
G5
D2
F2
D
Q
Clk
F1
D
Q
Clk
SYSTEM CLOCK
G3
G2
ADDRESS-DECODE LOGIC 42
En
D
Clk
R
A_to_B_Full 41
G4
D1
45
PROCESSOR A
Add
WS
Int
DATA

Fig.4.